REMARKS

By the Amendment, Applicants amend claims 1 and 11 and add new claims 21-23 to address other aspects of the present invention. Upon entry of this Amendment, claims 1-23 will be pending.

In the Office Action, the Examiner objected to claims 1 and 11 as containing informalities; rejected claims 1-3, 5-7, 11-13, and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,850,422 to Chen ("Chen"); rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of U.S. Patent Application Publication No. 2002/0030522 to Nakamura ("Nakamura"); rejected claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of U.S. Patent No. 7,113,560 to Huang et al. ("Huang")[1]; and rejected claims 10, 14, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of U.S. Patent Application Publication No. 2003/0061564 to Maddux ("Maddux").[2] Applicants respectfully traverse the Examiner's objection and rejection under § 103(a).

Regarding the claim objection

Applicants respectfully traverse the Examiner's objection to claims 1 and 11 as containing informalities. However, to expedite the prosecution of this application, Applicants have amended claims 1 and 11 to recite "the encoded phase transition data," as suggested by the Examiner. Accordingly, Applicants respectfully request withdrawal of the objection to claims 1 and 11.

---

[1] Applicants respectfully note rejections of claims 15 and 19 are discussed in the rejections of claims 9 and 8, respectively. Thus although claims 15 and 19 are not mentioned in the statement of any rejection, Applicants assume they are rejected under § 103 as unpatentable over Chen and Huang.

[2] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicants decline to automatically subscribe to any statement or characterization in the Office Action.

Regarding the rejection under 35 U.S.C. § 103(a)

Applicants respectfully traverse the Examiner's rejection of claims 1-3, 5-7, 11-13, and 16-18 under 35 U.S.C. § 103(a) as being unpatentable over Chen, because a *prima facie* case of obviousness has not been established.

To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* M.P.E.P. § 2142, 8th Ed., Rev. 5 (August 2006). Moreover, "in formulating a rejection under 35 U.S.C. § 103(a) based upon a combination of prior art elements, it remains necessary to identify the reason why a person of ordinary skill in the art would have combined the prior art elements in the manner claimed." USPTO Memorandum from Margaret A. Focarino, Deputy Commissioner for Patent Operations, May 3, 2007, page 2.

Independent claim 1, as amended, recites a combination including, for example, "an encoder, coupled to the half-rate phase detector, for encoding the phase transition data according to an optimum phase selected by the phase detector; and a confidence counter coupled to the encoder to receive the encoded phase transition data and provide an output representative of an accumulated effect of the phase transitions based on the encoded phase transition data." Chen fails to teach or suggest at least these features of amended claim 1.

The Examiner alleges that "Chen teaches of a method and a system comprising: . . . an encoder for encoding the phase transition data (#52, combinational logic, Fig. 6A, truth table, Fig. 6B); a confidence counter (#20, Fig. 1) coupled to receive the phase transition data (output from encoding in #18) and provide an output representative of an

accumulated effect (Col 1, line 67 to Col 2, Lines 1-5) of the phase transitions (Col 6, Lines 36-67 and Col 7, Lines 1-19)." (Office Action at 3.) Applicants respectfully disagree.

In the cited section, Chen explicitly states that "lead-lag phase detector 18 includes a plurality of D flip-flops 50 and combinational logic 52 which cooperate to produce LEAD and LAG output pulses which are eventually applied to the loop filter 20." Chen, column 6, lines 11-14. Therefore, in Chen, combinational logic 52 is only part of the lead-lag phase detector 18, and does not constitute "an encoder coupled to the half-rate phase detector for encoding the phase transition data according to an optimum phase selected by the phase selector," as recited in amended claim 1. In fact, Chen fails to mention any "optimum phase selected by the phase detector."

Further, Chen clearly states that "the lead-lag phase detector 18 eliminates the need for a known binary encoder thereby further reducing power consumption and chip area." Chen, column 6, lines 17-19, emphasis added. Thus, Chen actually teaches away from using a separate encoder to encode phase transition data.

Furthermore, Chen is completely silent on "an encoder, coupled to the half-rate phase detector, for encoding the phase transition data according to an optimum phase of the phase selector," as recited in amended claim 1 (emphasis added).[3] The Examiner alleges that "Applicant has not disclosed that a clock signal generated in half the rate of the transmitted serial data signal provides an advantage or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicants invention to perform equally well with providing a clock of the same frequency as the

[3] The Examiner concedes that "Chen does not teach of a clock signal generated in half the rate of the transmitted serial data signal." (Office Action at 4.)

data rate of the incoming data to reduce power consumption (Col 4, Lines 10-16)." (Office Action 4.)

Applicants respectfully disagree. Applicants in fact explicitly disclose the advantages of half of the rate clock signal in, for example, Description of the Related Art section of the specification that "[a] particular need exists in the art for a system and method overcoming disadvantages with respect to excessive power consumption and inefficient bandwidth use and difficulty in making fast data recovery decisions over a serial communication link." Also, "[i]n the case of noncontinuous data transmission, i.e., burst mode transmission, multi-rate oversampling with a long preamble may be required for data recovery. Such processing approaches in data transmission are disadvantageous because of their excessive power consumption and inefficient utilization of bandwidth over the communications link. Moreover, conventional CDR methods are not suited for making fast data recovery decisions." Specification, paras. [005]-[006], emphasis added. Applicants clearly indicate that half rate phase detectors have certain advantages.

Further, the Examiner is also not correct in stating "[o]ne of ordinary skill in the art, furthermore, would have expected Applicants invention to perform equally well with providing a clock of the same frequency as the data rate of the incoming data to reduce power consumption (Col 4, Lines 10-16)." (Office Action 4.) A full rate clock, i.e., a twice faster data rate, will certainly increase power consumption, not "reduce power consumption," which is among the disadvantages listed above.

Therefore, Chen fails to teach or suggest all elements of amended claim 1. A *prima facie* case of obviousness has not been established. Accordingly, Applicants

respectfully request withdrawal of the Section 103 rejection of amended claim 1. Because claims 2, 3, and 5-7 depend from claim 1, either directly or indirectly, Applicants also request withdrawal of the Section 103 rejection of claims 2, 3, and 5-7.

Further, amended independent claims 11 and 16, while of different scope, include similar recitations to those of amended claim 1. Claims 11 and 16 are therefore also allowable for at least the same reasons stated above with respect to claim 11. Applicants respectfully request withdrawal of the Section 103 rejection of amended claims 11 and 16 and claims 12-13 and claims 17-18, which depend from claims 11 and 16, respectively.

In addition, independent claim 16 recites a combination including, for example, "a clock for generating an 8-phase clock signal at half rate of transmitted serial data; [and] a half-rate phase detector for oversampling the transmitted serial data at four times the half clock rate and providing sampled data, and for detecting and grouping phase transitions between a phase lead and a phase lag in the sampled data and outputting phase transition data." (emphasis added) The Examiner concedes that "Chen does not disclose of oversampling the transmitted data at four times the sampling rate wherein the clock signal has eight phases for each period in the transmitted serial data." (Office Action at 4.)

However, the Examiner nevertheless alleges that "[i]t would have been an obvious matter of design choice to oversample the transmitted serial data at four times the rate of the transmitted serial data wherein the clock signal has ten phases for each period in the transmitted serial data." (Office Action at 4-5.) Applicants respectfully disagree.

Chen explicitly states that "[a]n input jitter tolerance of greater than 60% of the bit time is attainable with a 10X oversampling rate of the present invention. Thus, the input jitter tolerance obtained from a 10X oversampling rate is adequate." Chen, column 4, lines 38-42. Therefore, Chen strongly suggests using at least 10X oversampling rate, contrary to "a half-rate phase detector for oversampling the transmitted serial data at four times the half clock rate and providing sampled data," as recited in claim 16. Further, Chen fails to teach or suggest "a clock for generating an 8-phase clock signal at half rate of transmitted serial data," as recited in claim 16.

Applicants respectfully traverse the Examiner's rejection of claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Nakamura, because a *prima facie* case of obviousness has not been established.

Claim 4 depends from amended claim 1. As set forth above, Chen fails to teach or suggest at least "an encoder, coupled to the half-rate phase detector, for encoding the phase transition data according to an optimum phase selected by the phase selector; [and] a confidence counter coupled to the encoder to receive the encoded phase transition data and provide an output representative of an accumulated effect of the phase transitions based on the encoded phase transition data," as recited in claim 1 and required by claim 4.

Nakamura fails to cure the deficiencies of Chen. The Examiner alleges that "Nakamura teaches of an oversampling clock recovery circuit (title of invention) where a relatively small number of clocks are supplied, and controlled in phase by a phase control circuit." (Office Action at 6.) Even assuming the Examiner's allegation is

correct, which Applicants do not concede, Nakamura fails to teach or suggest at least the above listed elements recited in amended claim 1 and required by claim 4.

Therefore, neither Chen nor Nakamura, taken alone or in any reasonable combination, teaches or suggests all elements required by claim 4. A *prima facie* case of obviousness has not been established. Accordingly, Applicants respectfully request withdrawal of the Section 103 rejection of claim 4.

Applicants respectfully traverse the Examiner's rejection of claims 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Huang, because a *prima facie* case of obviousness has not been established.

Claims 8-10 depend from claim 1. Huang also fails to cure the above deficiencies of Chen. Huang teaches "[a] method and circuit to produce an optimal sampling phase for recovery of a digital signal." Huang, abstract. However, Huang fails to teach or suggest the above listed elements recited in amended claim 1 and required by claims 8-10.[4]

Therefore, neither Chen nor Huang, taken alone or in any reasonable combination, teaches or suggests all elements required by claims 8-10. A *prima facie* case of obviousness has not been established. Accordingly, Applicants respectfully request withdrawal of the Section 103 rejection of claims 8-10.

Applicants respectfully traverse the Examiner's rejection of claims 10, 14, and 20 under 35 U.S.C. § 103(a) as being unpatentable over Chen in view of Maddux. Claim

---

[4] As noted above, the Examiner appears to reject claims 15 and 19 while discussing the rejection of claims 8-10. See Office Action at 7-8. Because claim 15 depends from claim 11, and claim 19 depends from claim 16, Applicants respectfully submit that Huang also fails to cure Chen's deficiencies on teaching all elements of claims 11 and 16, as explained in previous sections. Thus, claims 15 and 19 are also allowable for at least being dependent on an allowable base claim.

10 depends from claim 1, claim 14 depends from claim 11, and claim 20 depends from claim 16. Applicants respectfully submit that Maddux also fails to cure Chen's deficiencies in teaching all elements of claims 1, 11, and 16, as explained in previous sections. Thus, claims 10, 14, and 20 are also allowable for at least being dependent on an allowable base claim.

Regarding the newly added claims

Applicants have added new claims 21-23 to address other aspects of the present invention. Support for new claims 21-23 may be found at, for example, pages 10-14 of the specification. Claims 21-23 are allowable at least due to their dependences from allowable claim 1. Further, the applied references fail to teach or suggest "wherein input data in the XOR logic gate have a phase transition rate twice of phase resolution of the phase detector," as recited in claim 21, "wherein XOR logic operation results are grouped into two sets according to sampled clock phases," as recited in claim 22, and "wherein the encoder encodes output data of the phase detector according to the optimum phase of the phase selector," as recited in claim 23.

Conclusion

In view of the foregoing amendments and remarks, Applicants respectfully request reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: September 28, 2007

By: _____
Wenye Tan /(571)203-2722
Reg. No. 55,662